|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **LEADLAG- in case of DC INPUT(slow dc with 100Hz & 50Hz frequency)** | | | | | | | |
| **Various Detected Faults in LEADLAG in the presence of faults with deviations (5% – 15%) & (20%-46%)** | | | | | | | |
| **Injected Faults** |  | **=500, = 5.1931e-04**  **Optimal Order – 14th** | | **=1000, = 5.1978e-04**  **Optimal Order – 14th** | | **=2000, = 5.2020e-04**  **Optimal Order – 14th** | |
| **No. of Coefficients Out of Bound** | **Fault Detection Status** | **No. of Coefficients Out of Bound** | **Fault Detection Status** | **No. of Coefficients Out of Bound** | **Fault Detection Status** |
| R1 12%  **↑** |  | 0 | **X** | 0 | **X** | 0 | **X** |
| R1 8%  **↓** |  | 0 | **X** | 0 | **X** | 0 | **X** |
| R2 9%  **↑** |  | 0 | **X** | 0 | **X** | 0 | **X** |
| R2 6%  **↓** |  | 0 | **X** | 0 | **X** | 0 | **X** |
| R3 10%  **↑** |  | 0 | **X** | 0 | **X** | 0 | **X** |
| R3 7%  **↓** |  | 0 | **X** | 0 | **X** | 0 | **X** |
| C1 13%  **↑** |  | 0 | **X** | 0 | **X** | 0 | **X** |
| C1 15% **↓** |  | 3 | **√** | 2 | **√** | 2 | **√** |
| C2 11% **↑** |  | 0 | **X** | 0 | **X** | 0 | **X** |
| C2 14% **↓** |  | 1 | **√** | 1 | **√** | 1 | **√** |
| R1 20%  **↑** |  | 1 | **√** | 0 | **X** | 0 | **X** |
| R1 30%  **↓** |  | 3 | **√** | 3 | **√** | 3 | **√** |
| R2 32%  **↑** |  | 1 | **√** | 1 | **√** | 1 | **√** |
| R2 40%  **↓** |  | 1 | **√** | 1 | **√** | 1 | **√** |
| R3 25%  **↑** |  | 10 | **√** | 8 | **√** | 8 | **√** |
| R3 45%  **↓** |  | 4 | **√** | 4 | **√** | 4 | **√** |
| C1 42%  **↑** |  | 4 | **√** | 4 | **√** | 3 | **√** |
| C1 25% **↓** |  | 2 | **√** | 2 | **√** | 2 | **√** |
| C2 35% **↑** |  | 0 | **X** | 0 | **X** | 0 | **X** |
| C2 47% **↓** |  | 35 | **√** | 30 | **√** | 26 | **√** |